IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

MICROUNITY SYSTEM ENGINEERING, INC., Plaintiff v. APPLE INC., et al., Defendant.	Case No. 2:10-cv-91-LED-RP Consolidated with Case No. 02:10-cv-185-LED-RSP JURY TRIAL DEMAND

DEFENDANTS' OBJECTIONS TO MAGISTRATE JUDGE PAYNE'S CLAIM CONSTRUCTION ORDERS [DKT. NOS. 544, 545] AND MOTION FOR RECONSIDERATION OF SAME

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES

Page

Cases

TABLE OF CONTENTS
(continued)

Page

Rules

I. INTRODUCTION

Pursuant to FED. R. CIV. P. 72 and L.R. CV-72, Defendants respectfully request that this Court reconsider and overrule the March 7, 2013 (D.I. 544) and March 8, 2013 (D.I. 545) Claim Construction Orders (the March 7 and March 8 Orders, respectively) entered by Magistrate Judge Roy S. Payne. Defendants object to each construction in the March 7 and March 8 Orders, except for "plurality of media data streams," on the bases set forth in Defendants' Responsive Claim Construction Briefs (D.I. 467 and 508), in the *Markman* Presentations attached as Exhibits A and B, in the transcript from the Markman Hearings, and for the reasons set forth below.

II. STANDARD OF REVIEW

Claim construction is a question of law. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 (Fed.Cir.1998) (en banc). A Magistrate Judge's claim construction findings and recommendations are subject to *de novo* review by the District Court. *Chiron Corp. v. Genentech, Inc.*, 266 F. Supp. 2d 1172, 1176 (E.D. Cal. 2002); L.R. CV-72(c).

III. ARGUMENT

A. The Construction Of "General Purpose Programmable Media Processor" ("GPPMP") Is Erroneous

Defendants respectfully submit that the March 7 Order errs in failing to adopt the disputed portions of Defendants' proposed construction of the GPPMP term. March 7 Order at 3-7. The primary claim construction dispute relates to whether a GPPMP can include "specialized media processing hardware." The teachings in the Asserted Patents exclude "specialized media processing hardware" because MicroUnity clearly and unambiguously disavow the use of specialized media processing hardware in favor of the claimed inventions (a general purpose programmable media processor). MicroUnity confirmed this disavowal during reexamination. This issue gets to the heart of MicroUnity's claimed invention: Defendants'

accused products—which use specialized media processors on the same chips as the accused processors—correspond to the "future of the old way" approach specifically disavowed by MicroUnity and distinguished from the claimed "single unified media processor" invention.[1]

1. I/O Blocks Are Not "Processing Hardware" and Are External to the GPPMP

In rejecting Defendants' construction, the March 7 Order notes that the specification makes references to "I/O" (input/output) blocks, such as the "Nyquist Sampled I/O" in Fig. 7, and I/O blocks for audio, video, and network in Fig. 19. March 7 Order at 4. The Order then states that this I/O circuitry "processes the data to some extent," concluding that the disclosed GPPMP includes specialized media processing hardware. *Id.* This is in error.

The cited I/O blocks are not specialized processors that *process* digital data: the GPPMP *processes* the data. The I/O blocks are input/output circuits that convert data into a digital format suitable for processing by the GPPMP. This distinction is conceded by MicroUnity. D.I. 443 at 8 ("The Nyquist sampled I/O … converts the analog media signals, such as audio, video, etc. – to digital signals that can be processed by the processor."). Thus, the Nyquist I/O is not "processing hardware" but merely a source of data that is processed by the GPPMP.[2]

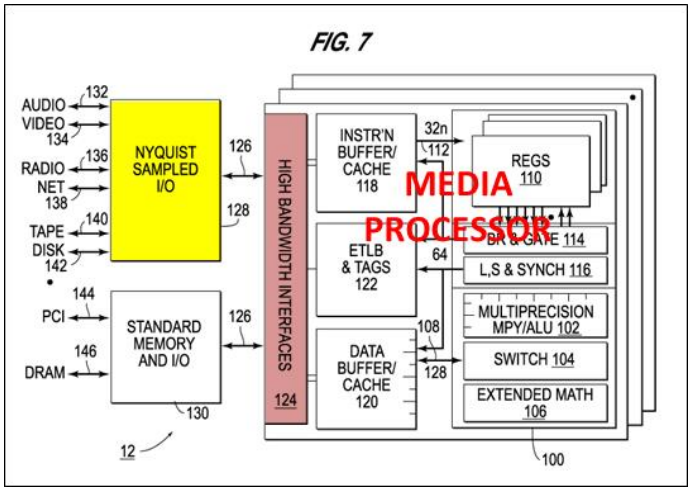
The specification distinguishes between input/output hardware and processing hardware by explaining that the media streams passing through the I/O hardware are processed, not by the

[1] *See, e.g.*, '840 patent Figure 5 and associated text, describing a system in which separate media processors are utilized, and this approach (the "old way") and disparaging and expressly distinguishing the claimed invention ("the unified way"). *See also id.* at 1:60-61 (stating that the "old way" has three fundamental flaws: cost, complexity, and rigidity") and 2:46-47 (stating the disadvantages of the old way "can be overcome by a single unified media processor"). *See also*, D.I. 467 at 2-9.

[2] As used in the Asserted Patents, "processing" refers to the digital processing of data and not to the conversion of data into a digital format for processing. *See, e.g.*, '840 Patent at 4:25-28 ("According to another aspect of the invention, a general purpose programmable media processor is provided having an instruction path and a data path to ***digitally process*** a plurality of media data streams.") (emphasis added).

I/O hardware, but by the GPPMP. '840 Pat. at 18:17-23 ("two basic forms of media data are processed by the general purpose media processor …. These data streams generally comprise Nyquist sampled I/O and standard memory and I/O.")

Additionally, the cited I/O blocks cannot be considered "specialized media hardware" within the GPPMP because the I/O blocks reside outside of the GPPMP. In the *Intel* case, MicroUnity referred to the Nyquist I/O as an "external device." *See* Case 2:04-cv-120, D.I. 117 at 47:14-48:8. The Asserted Patents also illustrate the Nyquist I/O as a block outside of the external interface (element 124) of the GPPMP:



'840 at Fig. 7; *see also id.* at Fig. 19 ("I/O Interfaces" are outside of "Processor"). Thus, it is error to characterize these I/O blocks as "processing hardware" within the GPPMP.

2. The Specification Does Not Teach Away From Defendants' Construction

Because the disclosed I/O blocks do not constitute specialized media ***processing*** hardware and are not a part of the GPPMP, the statement that "Defendants' assertions would conflict with teachings in the specification in which a processor may include specialized media circuitry for processing different media types in the I/O" is in error. March 7 Order at 5.

The March 7 Order also states that Defendants' construction would exclude the preferred

embodiment ("the unified way" of Figure 6) if additional specialized processor circuitry is added to the system because the claims use the "the open transition 'comprising'" preamble. March 7 Order at 5-6. This reasoning is flawed on multiple grounds.

First, while it is *presumptively* true that an "open" claim reads on devices including additional elements, this presumption evaporates when the patentee has disavowed a particular element. For example, in *BASF Agro B.V. v. Makhteshim Agan of North America, Inc.*, 2013 WL 1136714 (Fed. Cir. Mar. 20, 2013), the representative claim recited a process for applying termite spray "comprising … applying an effective amount of said solution or suspension to discrete locations around or under said building." The patentee asserted that this claim was open-ended and covers methods beyond the "discrete location" approach, including ones that use more solution to create a complete barrier. The Federal Circuit rejected this argument, noting that the patentee had disclaimed the "complete barrier" method by, among other things, highlighting its disadvantages in the specification and stating that the object of the invention was to "provide a termite treatment without barrier." The Federal Circuit then stated:

> [T]he claims' use of the open-ended term "comprising" is not sufficient to overcome Kimura's clear disavowal of certain subject matter. As we have said, "The open-ended transition 'comprising' does not free the claim from its own limitations." … Nor is "comprising" a talismanic incantation that counteracts a clear disclaimer. … We find Kimura's use of the word "comprising" insufficient to overcome the clear and definite disclaimer which is evident from the Kimura patents' text and prosecution history.

Id. at *9. Similarly, the specification of the Asserted Patents clearly disclaims the use of specialized media processing hardware. *See, e.g.*, '840 at 2:46-47 ("The disadvantages of the prior ASIC approach can be overcome by a single unified media processor."); *see also id.* at 3:44-47 ("It is also an object of this invention to achieve high bandwidth rates in a unified processor that is easy to program and more flexible than a heterogeneous ***combination of special purpose processors***.") (emphasis added); *see also* D.I. 467-2-9.

Though the March 7 Order does not dispute that Defendants' proposed construction is consistent with the specification, which repeatedly and consistently disparages the specialized media processor approach, it finds ambiguity in the intrinsic record based on statements made by MicroUnity in reexamination proceedings that purportedly contemplate some use of specialized media processors in conjunction with a general purpose media processor. March 7 Order at 6 (finding ambiguity based on "the intrinsic record" "taken as a whole"). The cited MicroUnity reexamination statements, however, involve the use of ***external*** specialized processors, not the internal specialized media processing hardware excluded under Defendants' proposed construction.[3] Accordingly, these statements do not create ambiguity with regard to the disclaimer of internal media processing hardware, and do not otherwise conflict with Defendants' construction. Moreover, a statement made in reexamination cannot create ambiguity and overcome a clear disclaimer in the specification. While a patentee's prosecution statements can ***limit*** claim scope, such statements cannot ***enlarge*** claim scope beyond those dictated by the specification. *Biogen, Inc. v. Berlex Labs., Inc.*, 318 F.3d 1132, 1140 (Fed. Cir. 2003) ("Representations during prosecution cannot enlarge the content of the specification."). Thus, when statements made by the patentee during prosecution conflict with the specification, the specification must control. *Aguayo v. Universal Instruments Corp.*, 356 F. Supp. 2d 699 (S.D. Tex. 2005) ("When the specification and the prosecution history conflict, any ambiguities must be resolved in favor of the specification and the claims."). Accordingly, reliance on these reexamination statements is inappropriate in light of clear specification disclaimer.

[3] For example, the March 7 Order cites the following reexamination statement discussing the relegation of operations to ***external*** processors: "The ability to dynamically partition integer and floating point data permits more efficient processor operation, and moreover, allows the designer to make strategic decisions about which operations are to be performed by the processor and which are to be ***relegated to peripheral processors or ASICS***." March 7 Order at 6 (citing '840 RE Resp. at 4, Dkt No. 433-32) (emphasis added).

3. The March 7 Order Errs In Rejecting the Phrase "one or more integrated circuit chips"

Defendants seek a construction of GPPMP that includes the phrase "one or more integrated circuit chips." The March 7 Order agrees that the processor can be "one or more integrated circuit chips," but states that the proposed language "appears to have the potential to create confusion for the jury." March 7 Order at 4. Defendants submit that GPPMP must be in the form one or more integrated circuit chips, and cannot be a portion of a chip. Thus, the proposed language is necessary to prevent MicroUnity from accusing a portion of a chip—such as the microprocessor 72 of the disclaimed "future of the old way" design shown in Figure 5—as the GPPMP while allowing specialized media processing hardware to exist on the same chip. Defendants' construction clarifies the issue for the jury.

B. The Construction of the Remaining "Processor" Terms Is Erroneous[4]

"The disputes raised with regard to the [remaining] processor terms are substantially the same as raised with regard to the [GPPMP term] … with the exception of two issues: (1) whether all the processor terms should be construed to have the same meaning requiring 'general purpose' and 'media' limitations, and (2) whether the preamble of the '765 patent is a limitation." *Id*. at 14. Defendants incorporate by reference their arguments and objections with regard to GPPMP set forth in Section III.A above. Moreover, Defendants submit that the March 8 Order errs in construing the processor terms to not include "general purpose" and "media," and that "programmable media processor" in claim 1 of the '765 is not a limitation.

Defendants' proposed construction for GPPMP is based on disavowals in the specification and file history distinguishing the claimed invention from prior art designs that include specialized media processing hardware. These disavowals limit the scope of the overall

[4] March 8 Order at 14-20.

invention and apply to all related claims directed at the processor of the alleged invention. D.I. 467 at 5-9. The Magistrate Judge's March 8 Order notes, but does not address, this argument.

The '840 Patent uses "general purpose, programmable media processor" (D.I. 443-2, '840 Patent at Abstract), "programmable media processor" (*id*. at 6:16), "general purpose programmable processor" (id. at 3:58-59), "general purpose processor" (*id*. at 7:28), "general purpose media processor" (id. at 8-1-2), and "media processor" (*id*. at 5:22) to describe the same processor. Similarly, the '765 Patent uses "programmable processor" (Dkt. 443-8, '765 Patent at Title, Abstract), "general purpose processor" (*id*. at 5:38, 9:16), "general purpose microprocessor" (*id*. at 2:1), and "programmable media processor" (*id*. at 42:58) interchangeably to describe or claim the same design. Other Asserted Patents are similar in this regard. These processor terms have the same meaning and therefore should have the same construction.

The March 8 Order states that a review of the '356, '765 and '131 Patents refutes Defendants' suggestion that the specifications only support claims to a "general purpose media processor." March 8 Order at 18-19. However, these patents claim priority to the '840 patent and similar terms should be construed consistently throughout a patent family. *See Omega Eng'g, Inc. v. Raytek Corp*., 334 F.3d 1314, 1334 (Fed. Cir. 2003) ("[W]e presume, unless otherwise compelled, that the same claim term in the same patent or related patents carries the same construed meaning."). Moreover, reference to these later filed patents to broaden the scope of the processor disclosed in the '840 Patent (i.e., no longer having to perform all operations necessary to be a GPPMP) is inappropriate due to MicroUnity's priority allegations to the '840 Patent. *See, e.g., MacLean-Fogg Co. v. Eaton Corp*., No. 2:07-cv-472, 2009 WL 2524595, * 9 (E.D. Tex. Aug. 14, 2009) ("Claims in a continuation application must be supported by the disclosures in the original specification.").

As for the '765 patent preamble and the use of "programmable media processor," the

March 8 Order agrees that a preamble may properly be considered a limitation, but concludes that "the claim in question provides a structurally complete claim and the limitations sought are not needed to give 'life, meaning and vitality' to the claims." March 8 Order at 20. But even a preamble in a claim that is structurally complete may be limiting if the patentee emphasizes the importance of the limitation to the claimed invention. *See, e.g., Hearing Components, Inc. v. Shure, Inc.*, 2008 U.S. Dist. LEXIS 121708, *9-10 (E.D. Tex. Dec. 16, 2008) (J. Clark) (preamble phrase cited in approximately half of the patent's claims "clearly intended … to be a limitation on the claims"). In this case, the applicants viewed "media processor" as essential and recited it in all 30 claims of the '765 Patent. The '840 Patent—from which the '765 Patent allegedly claims priority—uses "media processor" 156 times, and specifically uses "programmable media processor" once in the title, three times in the abstract, seven times in the summary of the invention, and five times in the description of the figures. D.I. 443-2 at Title, Abstract, and 1:20-7:61. This further demonstrates that the term "media processor" "discloses a fundamental characteristic of the claimed invention" and is therefore limiting. *See Poly-America L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004).

C. The Constructions of "Multi-Precision Execution Unit" and "Execution Unit" Are Erroneous[5]

Defendants object to the Magistrate Judge's constructions. The constructions elevate the role of claim differentiation beyond that envisioned by the Federal Circuit, permitting the doctrine to eclipse repeated definitions and disclaimers made in the specification and prosecution history that support Defendants' proposed construction. *See* D.I. 467 at 12-17 and 508 at 17-19; *see Retractable Tech., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011) ("any presumption created by the doctrine of claim differentiation will be overcome by a

[5] March 7 Order at 7-10 (addressing "multi-precision execution unit"); March 8 Order at 21-23 (addressing "execution unit").

contrary construction dictated by the written description or prosecution history").

MicroUnity clearly defined what it meant by an "execution unit." For example, in the '840 reexamination, MicroUnity stated: "the Specification … ***clearly defines*** the 'execution unit' as the 'core' of the media processor 12, including the ALU, switch and extended math element." D.I. 467-9, '840 RE 10/14/08 Amdt. at 11; *see also* D.I. 467 at 12-17 and 508 at 17-19. This is not a statement specific to any claim; it is a statement by the patentee in the intrinsic record explaining how the ***specification*** defines the "execution unit" term. *See Omega Eng., Inc.*, 334 F.3d at 1324 ("As a basic principle of claim interpretation, prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution.").[6]

In fact, MicroUnity had to define the specific structure of the execution unit during prosecution because the PTO found invalidity where, as here, the term is defined in purely functional language. *Compare* D.I. 467-8 at 31 (PTO interpreting "execution unit" broadly as "a unit that executes instructions") *with* D.I. 467-9 at 11 (MicroUnity arguing the "fallacy of such an overly broad interpretation" by the PTO). *See also* D.I. 467 at 16-17 and 508 at 19 (*citing, e.g., Halliburton Energy Serv., Inc. v. M-I LLC*, 514 F.3d 1244, 1255 (Fed. Cir. 2008) (for generic terms—terms without a specific structure known in the art—"defined in purely functional terms … [the Court should look to] context (e.g., the disclosure in the specification)" to determine the boundaries of the claim).[7]

For example, during reexamination, MicroUnity proposed a broad, structure-less

[6] Defendants also object to Magistrate Payne's rejection of the word "core" as ambiguous. D.I. 544 at 8. The word "core" is a commonly used term that would be familiar to the jury.

[7] MicroUnity admitted during prosecution that "execution unit" is a generic structure-less term: D.I. 508-12, '765 RE 5/2/06 Resp. at 46 (the claims "require[] an 'execution unit' that can perform certain operations but do[] not otherwise constrain the particular structure or circuitry that can be used. Rather, any hardware qualifies as an 'execution unit' so long as it can perform the claimed functions.").

Wikipedia definition for "execution unit" as "part of a CPU that *performs the operations and calculations* called for by the program." D.I. 467-9, '840 RE 10/14/08 Amdt. at 13. MicroUnity then asked the Examiner to look to the specification's definition of the structure for this term: "consistent with the above evidence the '840 patent describes that the portion of media processor (computer) 12 that performs operations specified by instructions is the multi-precision ALU 102, the switch 104 and the extended math unit 106, which make up the execution unit 100 as clearly described in the Specification of the '840 patent."). *Id.* MicroUnity continued this disclaimer by insisting that the "'840 patent specification provides 'enlightenment' regarding the meaning of the term 'execution unit.' As noted above, the PTO cannot ignore that guidance." *Id*. at 15. MicroUnity should not be permitted to rely on a clear structural definition of execution unit to get its patent allowed and then be able to step away from the structure and broaden its patent through functional language in court.

Defendants further object to the construction of "execution unit" as differing from the construction for "multi-precision execution unit." The patentee uses these terms interchangeably. *See* D.I. 508 at 17. The March 8 Order errs in not recognizing that the term "multi-precision execution unit" is just an amendment of the term "execution unit," and thus all definitional statements made to the latter apply to the former. March 8 Order at 23 (observing that the patentee was forced to amend the '840 patent's originally claimed "execution unit" to read a "multi-precision execution unit … utilizing simultaneous parallel processing."). *Compare Omega*, 334 F.3d at 1330 ("the doctrine of prosecution disclaimer is inextricably tied to the ***arguments, amendments or concessions*** made by the patentee during prosecution").

Defendants further object to the Magistrate's attempt to excise more than the "multi-precision" limitation out of the construction of "multi-precision execution unit" for the term "execution unit." "Precision" refers to the size of data; thus, "multi-precision" refers to the

capability of operating on more than one size of data. The Magistrate Judge's construction of "multi-precision execution unit" accounts for the multi-precision concept by including the terms "plurality of media data streams, each of a width up to the width of the data path." The March 8 Order notes that this language is the only language reflecting "multi-precision." March 8 Order at 22 ("In reply, MicroUnity asserts that the portions of the provisional construction it removed reflect 'multi-precision' insofar as it discusses the 'plurality of media data streams' ….). In construing "execution unit," instead of only excising the "multi-precision" portion of the construction, the Magistrate additionally excised the "simultaneous parallel" limitation. There is no rational reason espoused by any party to support removing this limitation.

D. The Construction of "Multi-Precision Arithmetic Unit" Is Erroneous

Defendants respectfully submit that the March 7 Order errs in failing to adopt the disputed portions of Defendants' proposed construction of "multi-precision arithmetic unit." March 7 Order at 10-13. "The only dispute is whether the arithmetic unit must be operable to perform each type of group operation at multiple precisions." *Id.* at 11.

Defendants object to the Magistrate Judge's construction for "multi-precision arithmetic unit" because it fails to account for disclaimer statements made during reexamination. In particular, MicroUnity argued to the PTO during reexamination that "[p]ursuant to the Court's Claim Construction Order [in *Intel*], the 'multi-precision' arithmetic unit must be capable of dynamic partitioning for addition, subtraction, multiplication, division, and other integer and floating point operations." D.I. 467-3, '840 RE 2/22/2007 Resp. at 23.[8] MicroUnity explicitly defined "dynamic partitioning" as "the ability of a processor to partition at one precision level (or data width) when executing one instruction, then switch to another precision level for the

[8] The title for this section of MicroUnity's response accords: "3. The MVP Does Not Include an Arithmetic Unit That Can Dynamically Partition Both Integer and Floating Point Values." *Id.* at 22.

next instruction if necessary." *Id.* at 10. MicroUnity also distinguished prior art during reexamination on the basis that it did not disclose a floating point operation capable of operating on data of different widths. *See id.* at 35 (arguing that the 88110 prior art does not meet the "multi-precision arithmetic unit" limitation because its "pcmp" instruction, even if a floating point operation, allegedly does not operate on data of different widths). *See Am. Piledriving Equip., Inc. v. Geoquip, Inc.*, 637 F.3d 1324, 1336 (Fed. Cir. 2011) (distinguishing prior art can serve as disclaimer). The Magistrate Judge erred by not considering this disclaimer evidence. *See* March 7 Order at 12-13 ("The only support Defendants' cite for their claim construction is the 'plain meaning' of the Intel construction, and a portion of the specification that the Court does not agree clearly supports limiting the claims as Defendants suggest.").

E. The Construction of "Dynamically Partitionable Arithmetic Unit" Is Erroneous

Defendants respectfully submit that the March 7 Order errs in failing to adopt Defendants' proposal that the "dynamically partitionable arithmetic unit" term should be given the same construction as "multi-precision arithmetic unit." March 7 Order at 13-16.

The Magistrate's construction fails to address the fact that the specification treats the "multi-precision arithmetic unit" and the "dynamically partitionable arithmetic unit" as the same unit. *See* '840 patent at Abstract, 2:58-65, 4:13-16. The Magistrate Judge did not explain why this evidence from the specification is not controlling, and did not cite any evidence that favors MicroUnity's proposed construction. Indeed, all evidence cited by the Magistrate supports Defendants' proposed construction.

Defendants further object to the Magistrate Judge's construction because it fails to limit the claim scope based on reexamination disclaimer statements. MicroUnity repeatedly equated "dynamically partitionable arithmetic unit" with "multi-precision arithmetic unit," and

distinguished prior art on this basis. *See* D.I. 671-11, '061 RE 6/22/07 Int. Sum. at 5, 14-15; D.I. 467-10, '061 RE 12/1/2008 Resp. at 32. The Magistrate Judge treated this as a "mistake" (March 7 Order at 16), even though MicroUnity consistently used the term "multi-precision arithmetic unit" in multiple filings with the PTO, and distinguished prior art during reexamination of the '061 patent by applying the definition of "multi-precision arithmetic unit"—which requires six specific operations—to the "dynamically partitionable arithmetic unit" term. *See'061* RE 2/22/07 Resp. at 32; '061 RE 6/22/07 Int. Sum. at 10; *id.* at 14-15.

The Magistrate Judge found that MicroUnity's reexamination statements "support finding that a 'dynamically partitionable arithmetic unit' ***must be*** capable of performing group multiply or divide operations." March 7 Order at 15 (emphasis added). The Magistrate Judge's construction, however, does not reflect the requirement of "group multiply or divide operation." Accordingly, if the Court does not adopt Defendants' original proposal, Defendants respectfully move for reconsideration of the "dynamically partitionable arithmetic unit" term and propose that the construction be "an arithmetic unit that can partition data into fields of variable width***, and is capable of performing group multiply and group divide operations***."

F. The Construction of "Partitioning a … Register" Is Erroneous[9]

The Magistrate Judge observed that the specification supports Defendants' proposal, with the exception of the inclusion of "*a variable number.*" March 7 Order at 20-21 (agreeing that MicroUnity's disclosed code "partitions 'full-width' 128-bit registers into separately accessible 128-bit or 64-bit read/write fields"). As such, Defendants alternatively offer a compromise construction proposal that this term means "dividing a register widthwise into [a variable number of] separately accessible read/write fields" (bracketed portion to be removed from construction). This proposed change accounts for proposals from both parties that dividing a register would

[9] March 7 Order at 20-21.

result in multiple fields[10], and clarifies the construction for the jury by identifying the required outcome of a "partitioning a … register" operation. This construction is important because, although MicroUnity dropped its initial proposal that "partitioning a register" means separating "the data" in a register, MicroUnity's experts contend that the current construction merely requires dividing ***the data*** stored in a register, and they do not mention separately accessible read/write fields.

G. The Construction of the 128-Bit Data Path Terms Is Erroneous[11]

The parties disagree whether "throughout" should be part of the construction. Defendants object to the construction of "the claimed data path has a width of 128 bits or more" because its ambiguity would permit MicroUnity to argue—as it has done in its expert reports—that two 64-bit buses collectively satisfy this limitation or that this limitation is met by a bus that has a 128-bit segment but is not 128-bits throughout.[12] Defendants note that in the March 7 Order, the Magistrate Judge recognizes that: "In other words, there must be at least one data path between the two elements described by the relevant surrounding claim language that has a width of ***128 bits or more along the length of the data path***." March 7 Order at 17 (emphasis added). The Magistrate Judge's clarifying statement implicitly acknowledges that the construed claim terms require a width of 128-bits or more along the length of—i.e. throughout—the claimed data path. Therefore, Defendants' proposed construction should be adopted.

[10] MicroUnity agreed that partitioning a register would result in "distinct fields" while Defendants further clarify that the outcome includes "separately accessible read/write fields."
[11] March 7 Order at 16-17.
[12] The March 7 Order notes that, at the Claim Construction hearing, MicroUnity conceded that it is "necessary that one of the data paths be 128 bits wide" and that the parties agreed that "if an accused device has a 128-bit wide bus and a 64-bit wide bus between two components, the claim is satisfied by the 128-bit wide bus." March 7 Order at 17.

H. The Construction of the "Elemental Width" and "Floating-Point Operations" Terms Are Erroneous[13]

The claim construction dispute is whether this claim term only requires specifying ***a*** width (as the Magistrate Judge adopted) or requires selecting "from ***several available*** [floating point] widths." The Magistrate Judge relies on claim differentiation to support its construction, but the law is clear that claim differentiation cannot overcome disclaimers in the specification and prosecution history. Defendants have proffered three different bases for disclaimer: (1) multiple widths are required for a key aspect of invention: "Multi-Precision;"[14] (2) the applicant taught multiple widths in its specification;[15] and (3) a single width was disavowed during prosecution. The March 7 Order does not address Defendants' first two bases.

Moreover, Defendants submit that the March 7 Order's conclusion regarding Defendants' third basis—prosecution disclaimer—is erroneous. MicroUnity distinguished the relevant claim ('217 Patent, claim 35) over the Agarwal prior art reference by stating that "Agarwal does not teach, disclose, or suggest that data in an operand register be partitioned into a ***variable*** number of data elements based on a ***dynamic*** elemental width specified in the same instruction for floating-point arithmetic operation." March 7 Order at 18 (emphasis added). This is an unequivocal admission that Claim 35 requires the availability of multiple elemental data widths

[13] The "Elemental Width" term is addressed in the March 7 Order at 17-18, while the "Floating Point" terms are addressed in the March 8 Order at 24-29.

[14] MicroUnity agrees multiple widths are required for multi-precision functionality, and that this functionality is an important aspect of the claimed invention. *See* D.I. 443 at 3 ("The MicroUnity processor was designed so that data could be partitioned into data elements having widths (e.g., 8, 16, 32, 64, or 128 bits) that varied on an instruction-by-instruction basis. . . . The ability of the MicroUnity processor to execute a wide range of group instructions on ***data of different types and widths***, and to do so dynamically on an ***instruction-by-instruction basis***, was a significant advance in the microprocessor industry ….") (emphasis added)

[15] The precision of the floating point value determines the width, and the patents teach multiple precisions. *See*, *e.g.*, D.I. 443-13, '217 at 34:25-30 (listing different operand sizes: half-precision (16) bits, single precision (32 bits), double-precision (64 bits), and quad-precision (128 bits)); '840 at 15:63-65 ("a floating point value can preferably be 16, 32, 64, or 128-bits wide").

as required under Defendants' proposed construction.[16]

Moreover, the March 7 Order does not address the portion of MicroUnity's Agarwal analysis in which MicroUnity expressly distinguished Agarwal on the ground that it did not allow selection of multiple element widths:

> Although Agarwal discloses obtaining single-precision and double-precision data elements, 'double-precision data elements are forwarded straight through" … and "***single-precision operands must be expanded*** so that each 32-bit element is placed at every 32-bit location in the data flow, padding each element with 32 zeros."

D.I. 467, Ex. 12 at 20 (emphasis added). As explained in oral argument, Agarwal only supported a single width of 64-bits. If operands were only 32-bits in size, the operands had to be expanded by adding zeros in front of the number until it was 64-bits wide. 11/30/12 Hr. Tr. at 89-90.

Similarly, with respect to the "Floating Point" terms, the March 8 Order states that the identified disclaimer statements "are more clearly directed toward distinguishing partitioning on an instruction by instruction basis rather than requiring multiple available widths for floating point operations."[17] March 8 Order at 28. The March 8 Order errs, however, in finding that there is "no clear disavowal ***that for every data type***, the execution unit must perform operations on multiple precisions." *Id.* at 28. This is incorrect because the claims at issue ('217 patent, claim 42; '806 patent, claims 1 and 10; and '765 patent claim 1) only recite the capability to perform ***floating point*** operations, and do not mention integer at all. Thus, the dynamic partitioning must be for the floating point operations. *See* Ex. B, slide 90 (citing '217 patent notice of allowance: "Examiner agrees with Applicant that Agarwal … do[es] not teach … partitioned into a variable number of data elements … and that such data elements are used in

[16] MicroUnity agrees that "dynamic partitioning" means "dividing widthwise into a variable number of elements." D.I. 414 [PR 4-3 JCC Statement] at p. 1.

[17] Similar to the agreed construction for "dynamic partitioning", the parties agree that "partitioning on an instruction by instruction basis" means "dividing data width-wise into a ***variable*** number of elements specified on an instruction by instruction basis." D.I. 506-15 at 3.

group floating point operations … (as described in claim 42)." *See also id.* at slide 88 (MicroUnity told PTO that '765 patent claim 1 covers "perform[ing] group floating point operations … that have been dynamically partitioned … [and that] claim 11 **adds** group integer operations to the capabilities of the media processor of claim 1" (emphasis added)).

The March 7 and March 8 Orders also dismiss the prosecution disclaimer by stating that the availability of multiple data widths was not the "focus" of MicroUnity's Agarwal argument. The Magistrate appears to be responding to MicroUnity's argument that a disclaimer is not effective if it was not relied upon. March 8 Order at 28. A disclaimer, however, exists whenever the patentee relies on a ground to distinguish prior art, whether or not the disclaimer forms the basis for the Examiner's action. *Am. Piledriving Equip.*, 637 F.3d at 1336 ("[W]e have made clear … [that] an applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well."); *Seachange Int'l, Inc. v. C-Cor, Inc.*, 413 F.3d 1361, 1374 (Fed. Cir. 2005) (an "applicant's argument made during prosecution may lead to a disavowal of claim scope even if the Examiner did not rely on the argument"). Thus, it does not matter whether the multiple-widths argument was the focus of MicroUnity's effort to distinguish Agarwal or a secondary argument. Moreover, the rebuttal presumption of claim differentiation cannot overcome the unambiguous Agarwal disclaimer statement. *See* D.I. 467 at 15-16 and 26 (*citing Retractable Tech., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011)).

I. The Construction of the Term "Group Floating Point Operations" Is Erroneous[18]

The parties dispute whether, as Defendants proposed, the construction for this term should include the term "SIMD" ("Single Instruction Multiple Data"). The March 7 Order states

[18] March 7 Order at 19-20.

that "the term [SIMD] appears to be susceptible to multiple meanings, which may lead to juror confusion …." March 7 Order at 19-20.[19] Instead of creating jury confusion, the inclusion of the term SIMD would better align this construction with the Asserted Patents, which use the terms "group operation" and "SIMD" interchangeably. *See* '287 Patent at 9:19-22; '806 Patent at 9:19-22; '973 Patent at 9:19-22 ("Group or SIMD (single instruction multiple data) operations sustain external operand bandwidth rates up to 512 bits …."). Moreover, the adopted construction does not explain that the "group floating point operations" in question are, as MicroUnity concedes (D.I. 443 at 2), ***single instructions*** that are applied to a group of operands. The inclusion of the word "SIMD" (perhaps followed by "single instruction multiple data") would cure this defect.

J. The Construction of "Registers" Is Erroneous[20]

The March 7 Order states that: "The Court rejects Defendants contention that reading 'a register' means reading one and only one register." March 7 Order at 21. Defendants object to this statement.[21] In addition, Defendants object to the construction as it does not resolve a fundamental dispute between the parties, whether the claimed "register" encompasses software logically treating two separate registers as a single register-pair. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co*., 521 F.3d 1351, 1360 (Fed. Cir. 2008) ("the court, not the jury, must resolve [claim construction] dispute").

First, the Magistrate Judge errs by ignoring that the specifications refer to and define "registers" and "register pairs" as two separate things. *See, e.g.*, March 8 Order at 32 ("the result

[19] It appears that the Magistrate Judge was persuaded by MicroUnity's argument that "SIMD" has been used, on some occasions, to describe a multiprocessor system. D.I. 443 at 22. Defendants have expressly stated that their proposed construction "does not impose a multi-processor requirement on the execution hardware." D.I. 467 at 27.

[20] *See* March 7 Order at 21-22. The "register" construction is also addressed in the March 8 Order at 29-33.

[21] Defendants observe, however, that this statement does not appear to be part of the construction for this term. *See* March 7 Order at 21 (noting construction in bolded language).

is placed in the register *or register pair* specified ….") (citing "'840 Pat. Appendix" at 106). If the patentee had intended the claims to cover registers pairs, it should have stated such. Instead, the specifications note the significant drawbacks in designs that use register-pairs instead of a single wide register. D.I. 467 at 28 ("[t]he use of register pairs creates an undesirable complexity") (citing '356 patent at 22:20-47).

Second, the Magistrate Judge errs in finding that Defendants' proposed construction would exclude the preferred embodiment. The Magistrate Judge cited pseudocode in the '840 "Appendix" as supporting a preferred embodiment. March 7 Order at 22. This cited pseudocode, however, only establishes that a certain embodiment is capable of reading from *two separate* registers: "REG[rn+1]" and "REG[rn]." It is not disputed that the patents disclosed operations on single registers and operations on register pairs. Each claim needs not cover both the "register" and "register pair" embodiments. *See Sinorgchem Co. v. ITC*, 511 F.3d 1132, 1138 (Fed. Cir. 2007) ("A patent claim should be construed to encompass *at least one* disclosed embodiment in the written description portion of the patent specification.") (emphasis in original; citation omitted).

Third, the Magistrate Judge errs by discounting express disclaimers that "a register" cannot encompass register-pairs. MicroUnity overcame the Watkins prior art reference by arguing that Watkins uses shift instructions to operate on "separate register, not data elements catenated in *an* operand register."[22] This disclaims "register" from encompassing register-pairs, because Watkins disclosed using an instruction to read data out of more than one register, i.e., a register-pair. *Compare* March 7 Order at 21 (the "Court rejects Defendants contention that reading "a register" means reading one and only one register").

Lastly, the Magistrate Judge also errs by misapplying the general patent law maxim that

[22] *See* March 8 Order at 31 (discussion regarding "catenated data").

the "plain and ordinary meaning of the article 'a' is one or more." *See* March 8 Order at 32. Typically, in the context of an open-ended "comprising" claim, infringement can be found when there is one or more of the recited structure. This general rule, however, does not apply when "the claims and written description … make clear that the singular meaning applies." *TiVo, Inc. v. EchoStar Communications Corp.*, 516 F.3d 1290, 1303 (Fed. Cir. 2008). Here, the singular meaning of "a register" should apply in light of the patents referring to registers and register-pairs as two separate things, and in light of the specification and prosecution history disclaimers regarding register-pairs. Additionally, Defendants do not contend that simply adding an additional register creates non-infringement. Instead, Defendants only contend that the claimed recitations of partitioning, or returning results to, "a register" should be interpreted in the singular consistent with the plain claim language.

K. The Construction of "Subfield" Is Erroneous

The primary dispute between the parties relates to whether the term "subfield" refers to a field smaller than the full field size. March 7 Order at 23-24.

The only evidence in the specification discussing the term "subfield" uses this term to refer to less than the full field size, as proposed by Defendants. *See* March 7 Order at 23 (citing '840 Patent at 12:19-22, 12:25-27; Fig. 8B). The Magistrate Judge improperly relied upon the purported "Appendix" to the '840 patent in rejecting the Defendants' proposed construction. *See* March 7 Order at 24. First, the Appendix never mentions the term "subfield" and therefore cannot override the patentee's usage of the term in the specification. Second, the Appendix is not part of the '840 patent specification for purposes of claim construction because it is a microprocessor architecture specification that does not fall within the set of materials permissible for attachment as an Appendix. *See* 37 C.F.R. § 1.96. Thus, the Magistrate Judge's reliance on this evidence cited by MicroUnity is not proper.

The Magistrate Judge also accepted a dictionary definition cited by MicroUnity, but reliance upon this dictionary definition is improper for two reasons. First, dictionary definitions cannot trump the patentee's usage of a term in the specification. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005). Second, the dictionary definition cited by MicroUnity is not even the same term that is being construed. The term at issue is "subfield," and the dictionary definition relied upon by the Magistrate Judge is "subset." March 7 Order at 23. Thus, the Magistrate Judge's reliance on the plain and ordinary meaning for the term "subfield," as established by a dictionary definition for a different word, is in error.

L. The Construction of "High Bandwidth External Interface" and All Related Terms Are Erroneous[23]

The parties' dispute can be summarized as follows: MicroUnity contends that interface bandwidth can be a small fraction of execution unit throughput, while Defendants contend that the "high bandwidth" term requires an interface having bandwidth comparable to peak data throughput of the processor. The Magistrate Judge largely agreed with MicroUnity and found that "high bandwidth external interface" means "an interface between the media processor and external sources of data," and that the "maintains peak operation" terms mean "capable of transferring data at a rate that maintains the operation of the execution unit of the media processor at or near the maximum number of operations per unit time that the execution unit is capable of processing." March 8 Order at 10. Defendant submit that this is clear error.

First, the Magistrate Judge's construction of "high bandwidth external interface"—"an interface between the media processor and external sources of data"—simply reads out the "high bandwidth" term as a claim limitation. It is almost never appropriate to read out express claim language. *See, e.g., Dayco Products, Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1369 (Fed.

[23] March 8 Order at 4-14.

Cir. 2003) (error when court's claim construction read out claim term expressly recited in the body of the claim); *Texas Instruments Inc. v. United States Int'l Trade Comm'n*, 988 F.2d 1165, 1171 (Fed. Cir. 1993) (express limitations cannot properly be read out of the claims through claim construction). The March 8 Order states that "it is not necessary to specify a rate constraint within the construction of this term because surrounding limitations in the claims where the 'high bandwidth external interface' term appears specify the rate constraint" (*id.* at 10) and treats "high bandwidth" as mere surplusage. "All the limitations of a claim must be considered meaningful" and should be given effect. *Cablestrand Corp. v. Wallshein*, 29 F.3d 644 (Fed. Cir. 1994). Claim constructions that treat an express limitation as mere surplusage should be rejected. *Id.; Dayco Products, Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1369 (Fed. Cir. 2003).

Second, Defendants' construction is consistent with the patent disclosures. The adopted construction, which eliminates any distinction between a high bandwidth interface and any other interface, is not. For example, all "media processors" require an external interface; however, only 4 of 20 asserted claims require a "high bandwidth" interface. This demonstrates that the applicants viewed a "high bandwidth" interface as a specific subset of all possible interface types. Consistent with this, the intrinsic record discloses embodiments having a wide range of interface bandwidths. *See, e.g.*, '061 at 12:8-17, 18:52-57, and 20:54-57. The March 8 Order also errs by stating that Defendants did not cite evidence "support[ing] their assertion that the interface and the execution unit may cycle at different rates." May 8 Order at 11. Defendants cited a portion of the patent appendix explaining that the clock frequencies of the processor ("PLL0") and interface ("PLL1") are independently controlled by different "frequency

generators." Ex. B at 15 (citing to D.I. 508, Ex. 9 at 208).[24]

Third, the Magistrate Judge's construction of the "maintains peak operation" term impermissibly broadens the scope of the claims at issue. Defendants submit that the word "maintain" needs no construction, and there is no reason to expand "***maintain***" into "capable of transferring data at a rate that ***maintains***."

Fourth, the Magistrate Judge errs in concluding that "the mere fact that the *Intel* court's construction was presented to the Patent Office does not help the Court resolve the present dispute." March 8 Order at 12. The Magistrate Judge asserts that "Defendants do not point to any part of the prosecution history where MicroUnity relied upon or advocated for the use of this particular construction" and "the mere disclosure of a claim construction opinion does not operate as a disclaimer." *Id.* There is no need, however, for Defendants to cite specific portions of the prosecution history when MicroUnity has conceded that it asked the PTO to adopt ***all*** of Judge Ward's constructions. *See* D.I. 508-8 (8/16/12 Hearing Tr.) at 6:20-7:1 (MicroUnity argued: "And finally and most importantly and underlying all of our arguments today … is the simple fact that MicroUnity put before the Patent Office ***all of Judge Ward's constructions*** and repeatedly and consistently during re-examination ***urged their adoption***.") (emphasis added). Having relied on its embrace of Judge Ward's constructions to obtain favorable constructions in the first round, MicroUnity is judicially estopped from disavowing any of these instructions now.

Finally, the Magistrate Judge errs in permitting MicroUnity to depart from agreements reached on proposed constructions earlier in the claim construction process. MicroUnity had every opportunity to craft its initial constructions as it wished, and has failed to point to any

[24] As explained above in Section III.K, Defendants contend that the Appendix was improperly incorporated under 37 C.F.R. § 1.96. However, to the extent that MicroUnity relies on the Appendix for claim construction, it discloses that the processor and interface are independently controlled.

ambiguity in those constructions that would justify re-opening argument. The March 8 Order states that "Defendants will not be prejudiced by MicroUnity's changed position." Defendants have been prejudiced by MicroUnity's late reversal in the claim construction process (in September 2012, after the first Markman hearing), after it had received favorable constructions in the first round of claim construction based, in part, on its purported embrace of all of Judge Ward's constructions (including those it now seeks to disavow). Under these circumstances, prejudice is inherent. This Court recently rejected a similar attempt by a party to alter the construction of a previously agreed-on term. *See Soverain Software LLC v. J.C. Penney Corp.*, Case No. 09-CV-00274 (E.D.Tex. Oct. 20, 2011). It should follow suit here.

M. The Construction of "Catenated Result" and "Unified Symbol Field" Are Erroneous[25]

Defendants object to the constructions for "catenated result" and "unified symbol field" to the extent that the constructions encompass interpreting claims that recite returning catenated results to ***a*** register as encompassing returning catenated results to a register pair. Defendants incorporate their objections and arguments for the "register" term discussed herein.

N. The Construction of "Computer System" Is Erroneous[26]

The parties dispute whether the claimed computer system must include a "programmable processor" (as that term is construed by the Court). The relevant claims recite a "computer system" that includes an execution unit for performing partitioning and specific group operations. The asserted patents ***repeatedly*** disclose that this execution unit is part of a programmable processor. *See, e.g.*, D.I. 443-21, 22 ['287 Pat.] at Abstract ("Methods and software are presented for processing data in a programmable processor … using an execution unit operable to execute instructions by partitioning data … [the] instruction set includes group

[25] March 8 Order at 29-33.
[26] March 8 Order at 36-37.

arithmetic instructions and data handling instructions"); *see also* D.I. 508 at 29-30.

The Court erred by focusing too heavily on the claim language without the context of the specification. When a specification ***repeatedly*** reinforces the usage of a term, the claims cannot be of broader scope than the invention. *See On Demand Mach. Corp. v. Ingram Indus., Inc*., 442 F.3d 1331, 1340 (Fed. Cir. 2006). Here, there is no disclosure of any other structure that could contain this execution unit. Thus, the Magistrate Judge's construction allows the claims to be read broader than the invention disclosed, creating indefiniteness problems.

This error is compounded because it allows the patentee to avoid the structural limitations, created by the express disavowals noted herein, imposed in the construction of "programmable processor"—without requiring the patentee to teach the public any other way to implement the disclosed invention in a way that does not require these structural limitations.

IV. CONCLUSION

For the above reasons, Defendants respectfully request that the Court reconsider and overrule the March 7 and March 8 Orders.

Dated: April 1, 2013

/s/ Mark E. Miller, with permission by Michael E. Jones
Michael E. Jones
mikejones@potterminton.com
Allen F. Gardner
allengardner@potterminton.com
Potter Minton, P.C.
110 North College, Suite 500
P.O. Box 359
Tyler, TX 75710
Telephone: (903) 597-8311
Fax: (903) 593-0846

George Riley
griley@omm.com
Mark E. Miller
markmiller@omm.com
Ryan K. Yagura
ryagura@omm.com
Xin-Yi Zhou
vzhou@omm.com
O'Melveny & Myers LLP
Two Embarcadero Center, Suite 2800
San Francisco, CA 94111
Telephone: (415) 984-8700
Fax: (415) 984-8701

Attorneys for Samsung Electronics Co., Ltd.; Samsung Semiconductor, Inc.; and Samsung Telecommunications America, LLC

/s/ Michael R. Rueckheim by Permission
David J. Healey
healey@fr.com
John Philip Brinkmann
brinkmann@fr.com
Michael R. Rueckheim
rueckheim@fr.com
Fish & Richardson, PC
1221 McKinney Street, Suite 2800
Houston, TX 77010
Telephone: (713) 654-5300
Fax: (713) 652-0109

Katherine K. Lutton
lutton@fr.com
Kelly C. Hunsaker
hunsaker@fr.com
Shelley K. Mack
mack@fr.com
Fish & Richardson, PC
500 Arguello St., Ste 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Fax: (650) 839-5071

Eric M. Albritton
Texas State Bar No. 00790215
ema@emafirm.com
Albritton Law Firm
P.O. Box 2649
Longview, TX 75606
Telephone: (903) 757-8449
Fax: (903) 758-7397

Attorneys for Apple Inc.

/s/ Christopher Lawnicki by Permission
David A. Nelson
davenelson@quinnemanuel.com
Christopher Lawnicki
chrislawnicki@quinnemanuel.com
Quinn Emanuel Urquhart & Sullivan LLP
500 W. Madison St., Suite 2450
Chicago, IL 60661
Telephone: 312-705-7400

/s/ Indranil Mukerji by Permission
Michael J. McKeon
mckeon@fr.com
Indranil Mukerji
mukerji@fr.com
FISH & RICHARDSON P.C.
1425 K Street, NW, Suite 1100
Washington, DC 20005
Telephone: (202) 783-5070

Fax: 312-705-7401

Jennifer A. Kash
jenniferkash@quinnemanuel.com
Linda Brewer
lindabrewer@quinnemanuel.com
Derek Tang
derektang@quinnemanuel.com
Keala Chan
kealachan@quinnemanuel.com
Quinn Emanuel Urquhart & Sullivan LLP
50 California St., 22nd Floor
San Francisco, CA 94111
Telephone: 415-875-6600
Fax: 415-875-6700

Harry L. Gillam, Jr.
gil@gillamsmithlaw.com
Gilliam & Smith LLP
303 South Washington Avenue
Marshall, TX 75670
Telephone: 903-934-8450
Fax: 903-934-9257

Attorneys for Qualcomm Inc.

/s/ Kyle Chen by Permission
Thomas J. Friel, Jr.
tfriel@cooley.com
Heidi L. Keefe
hkeefe@cooley.com
Mark R. Weinstein
mweinstein@cooley.com
Kyle Chen
kyle.chen@cooley.com
Jason Fan
jfan@cooley.com
Lam K. Nguyen
lnguyen@cooley.com
Cooley LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155
Telephone: (650) 843-5000
Fax: (650) 849-7400

Robert W. Weber

Fax: (202) 783-2331

Keeley I. Vega
kvega@fr.com
FISH & RICHARDSON P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Fax: (650) 839-5071

J. Thad Heartfield
thad@jth-law.com
M. Dru Montgomery
dru@jth-law.com
The Heartfield Law Firm
2195 Dowlen Road
Beaumont, TX 77706
Telephone: (409) 866-3318
Fax: (409) 866-5789

Attorneys for LG Electronics MobileComm USA, Inc., LG Electronics, Inc.

/s/ Tyler T. VanHoutan by Permission
Jennifer Parker Ainsworth
jainsworth@wilsonlawfirm.com
Wilson, Robertson & Cornelius, P.C.
P.O. Box 7339
Tyler, TX 75711
Telephone: (903) 509-5000
Fax: (903) 509-5092

Tyler T. VanHoutan
tvanhoutan@winston.com
Michael J. Forbes
mforbes@winston.com
Winston & Strawn LLP
1111 Louisiana, 25th Floor
Houston, Texas 77002-5242
Telephone: (713) 651-2600
Fax: (713) 651-2700

Attorneys for Google Inc.

bweber@smithweber.com
Smith Weber, LLP
5505 Plaza Drive
P.O. Box 6167
Texarkana, TX 75505-6167
Telephone: (903) 223-5656
Fax: (903) 223-5652

Attorneys for HTC Corporation, HTC America, Inc., and Exedea, Inc.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on April 1, 2013.

/s/ Michael E. Jones